The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

I. Drawing Objections are Obviated

In paragraph 3, the Office Action objects to Figs. 24, 25, and 26A-26C. As set forth in the attached Request for Approval of Drawing Corrections, Figs. 24 and 25 are proposed to be labeled with "related art"; and Figs. 26A-26C are proposed to be labeled with "Prior Art". Applicants respectfully submit that Figs. 24 and 25 not only indicate that which is old (specification, page 1, lines 17-22), but Figs. 24 and 25 also depict the present invention (specification, page 7, lines 32-33). Withdrawal of the objection to Figs. 24, 25 and 26A-26C is respectfully solicited.

II. The Claims Define Allowable Subject Matter

The Office Action rejects claims 1-6, 8-10, 12-16 and 18-25 under 35 U.S.C. §103(a) over U.S. Patent 5,824,186 to Smith et al. (hereinafter "Smith") in view of alleged Prior Art Admissions. This rejection is respectfully traversed.

Smith does not teach, disclose or suggest "memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the microstructure; ... the peripheral circuit being separately formed on the substrate," as recited in claims 1-3 and 8-10; and as similarly recited in claims 12-14, 18 and 19. Instead, Smith discloses microstructures aligned into recessed regions of a substrate such that the microstructure becomes integral with the substrate.

The alleged Prior Art Admissions do not make up for these deficiencies. Instead, the Background of the Invention of the specification discloses that such a conventional ferroelectric memory is fabricated by integrating the passive matrix array and the peripheral circuits on a single substrate (page 1, lines 24-27). Such conventional art of common formation of a MOS transistor which makes up the peripheral circuits (Fig. 26A; page 1, lines 28-32) and the formation of the passive matrix array (Fig. 26B; page 2, lines 15-23) on a

single common substrate shows compromised deteriorations (page 2, lines 21-22) in the quality of the fabrication process output. The alleged Prior Art Admissions do not teach, disclose or suggest the claimed feature of the passive matrix array and the peripheral circuits being separately fabricated, with support for the claimed feature found on page 8, lines 31-32.

For at least these reasons, a combination of Smith and alleged Prior Art Admissions does not render obvious the subject matter of claims 1-6, 8-10, 12-16 and 18-25 under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 1-6, 8-10, 12-16 and 18-25 under 35 U.S.C. §103(a) over Smith in view of alleged Prior Art Admissions is respectfully requested.

III. Conclusion

For at least the reasons discussed above, it is respectfully submitted that this application is in condition for allowance.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

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JAO:RJK/sld

Attachments:
Petition for Extension of Time
Appendix
Request for Approval of Drawing Corrections

Date: December 9, 2002

APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claims:

1. (Twice Amended) A ferroelectric memory, comprising:

a microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the microstructure;

a substrate, the microstructure being integrated on the substrate; and

a peripheral circuit for the passive matrix array, the peripheral circuit being separately formed on the substrate.

2. (Twice Amended) A ferroelectric memory, comprising:

a substrate;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the substrate;

a microstructure; and

a peripheral circuit for the passive matrix array, the peripheral circuit being separately formed on the microstructure, the microstructure being integrated on the substrate.

3. (Twice Amended) A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;

a second microstructure;

a peripheral circuit for the passive matrix array, the peripheral circuit being separately formed on the second microstructure; and

a substrate, the first and second microstructures being integrated on the substrate.

8. (Twice Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors;

a peripheral circuit for the passive matrix array;

an associated circuit having a same or a different function as the memory cells;

a single substrate; and

a plurality of microstructures, the passive matrix array, the peripheral circuit and the associated circuit being separately formed on each of the plurality of microstructures, the microstructures being integrated on the single substrate.

9. (Twice Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors;

a peripheral circuit for the passive matrix array; and

a single microstructure, the passive matrix array and the peripheral circuit being separately fabricated and integrated on the single microstructure.

10. (Twice Amended) A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on the first microstructure;

a second microstructure that is larger than the first microstructure, the first microstructure being provided in a part of the second microstructure to be integrated; and

a peripheral circuit for the passive matrix array, the peripheral circuit being separately formed on the second microstructure.

12. (Twice Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on a microstructure;

separately forming the peripheral circuit on a substrate; and

integrating the microstructure on the substrate.

13. (Twice Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on a substrate;

separately forming the peripheral circuit on a microstructure; and

integrating the microstructure on the substrate.

14. (Twice Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure; and

integrating the first and second microstructures on a substrate.

18. (Twice Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure which is larger than the first microstructure; and

providing the first microstructure in a part of the second microstructure to be integrated.

19. (Twice Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

separately forming the passive matrix array on each of a plurality of microstructures; and

providing the microstructures in layers to be integrated in a substrate.